Analysis and Design of an Isolated Single-Stage Three-Phase Full-Bridge with Current Injection Path PFC Rectifier for Aircraft Application

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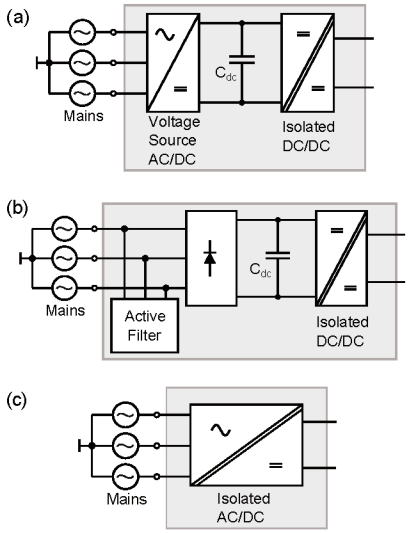

Figure 1: (a) two-stage rectifier system. (b) diode-bridge rectifier with active filter + isolated DC/DC stage. (c) single-stage isolated AC/DC converter.

I. Introduction

During the last decade, the More Electric Aircraft (MEA) concept has been gaining more and more focus both in the civil and military aircraft world [1]. This results from the replacement of pneumatic, mechanic, and hydraulic actuators by electric actuators. Thus the maintenance effort of the system is reduced and also energy conversion becomes more efficient.

All these innovations have increased the demand of electrical power in airplanes, which has prompted the incorporation of a new level of distribution power in military aircrafts. The classical aircraft distribution is a three-phase grid with 115 V ac at 400 Hz and output at 28 V dc. The new high DC voltage distribution is 270 V dc. The main advantage is that by decreasing the current level to 10 times lower than the traditional low voltage, the weight of the cabling is reduced [2], [3].

Generally speaking, an isolated three-phase AC/DC rectifier system can be achieved by : a) an active PFC rectifier stage + an isolated DC/DC stage [4]; b) a diode bridge with active power filter AC/DC stage + an isolated DC/DC stage; c) an isolated single-stage AC/DC rectifier (see Fig. 1). In (a), the complete power has to be processed through two stages, leading to high losses and thus low efficiency. However in (b), The active power filter only needs to process a small amount of total power. In this way, the global efficiency can be increased but still depends on high number of semiconductors, which is prone to lower reliability. In order to obtain high efficiency, high power density and high reliability (i.e. low number of controlled semiconductors), the emergence of isolated single-stage topology is advantageous [5].

In [6] an isolated matrix-type rectifier inheriting the operating principle of full-bridge is proposed, with the merit of Zero Voltage Switching (ZVS) and single-stage isolation. It has large number of semiconductors and modulation complexity. In [7], an isolated single-stage topology is presented based on a two-switch three-phase rectifier. This topology is easy to control and it operates in discontinuous conduction mode (DCM). Thus it shows higher RMS current which can be useful for high frequency low-medium power application. An isolated single-stage Swiss-Forward topology is proposed in [5], showing lower number of high frequency transistors but higher voltage stress on semiconductors because of the forward structure.

Later proposed in [8], the rectifier stage of the I^2AFM PFC rectifier consists of a passive three-phase diode bridge rectifier with an additional injection circuit: the integrated active filter (IAF), comprising a high-frequency bridge-leg with the switches S_1 and S_2, the inductance L and the low-frequency bidirectional switches S_a, S_b and S_c. In order to

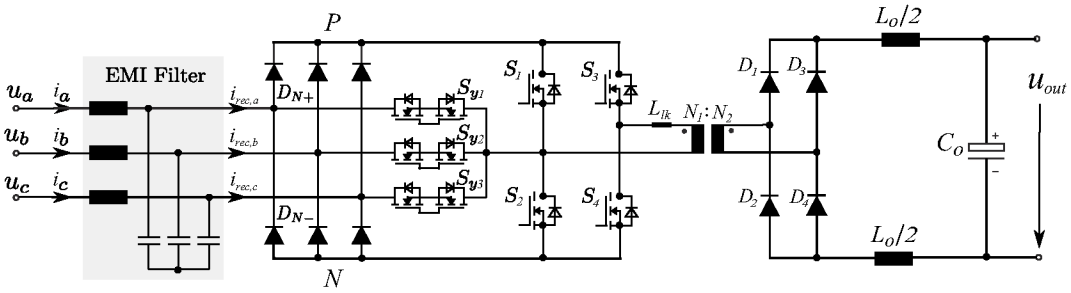

Figure 2: Proposed topology of an isolated single-stage three-phase full-bridge with current injection path PFC rectifier (IS^{2}FBCIP PFC Rectifier).

achieve sinusoidal input currents shape from the mains, the two switches on the half-bridge leg of the injection circuit can be controlled in such a way that a third harmonic current is forced into the phase with the smallest input absolute voltage. Besides, since the intermediate bus voltage will not be constant but vary with a sixfold mains-frequency, the phase shift in the full-bridge operation has to be adjusted to obtain a constant dc output voltage, meanwhile providing isolation. Also, a capacitor is placed in between two stages to decouple the functionality.

Based on the I^{2}AFM PFC rectifier, an isolated single-stage three-phase full-bridge PFC rectifier with current injection path is proposed in this paper (denominated as IS^{2}FBCIP PFC Rectifier), shown in Fig. 2. This topology is an isolated single-stage rectifier, and it has ZVS feature since the full-bridge operation (by MOSFETs S_1, S_2, S_3, S_4) is integrated. Each component on the current injection path (S_{y1}, S_{y2} and S_{y3}) needs to be a bidirectional switching pair since it has to present a four-quadrant behavior. On the secondary of the transformer, a diode bridge rectifier and L-C output filter are used to reach a constant output voltage u_{out}. Compared to I^{2}AFM PFC rectifier, less semiconductors are used, ZVS can be reached for all the semiconductors, and also the decoupling capacitor and current injection inductor are removed in the proposed topology, leading to higher efficiency and more compact design.

In Section II, the operating principle and modulation method of IS^{2}FBCIP PFC rectifier are discussed including the description of ZVS realization. In Section III, a design guideline is presented for a demonstrator prototype with output power rating of 3.3 kW, simulation results are provided to validate the functionality of the converter topology. The prototype hardware design parameters are finally described in Section IV.

II. Operating Principle and Modulation Method

The operating principle of the proposed rectifier shows similarity with I^{2}AFM PFC Rectifier, being different that the operation of the current injection path is integrated into the operation of the phase-shifted full-bridge.

A. Operating Principle

To demonstrate the operating principle of the proposed rectifier, 12 sectors of the mains phase voltage are divided and shown in Fig. 3. Here sector 1 (where $u_a > 0 > u_b > u_c$) is used for example. As shown in Fig. 4, u_{prim} depicts the voltage

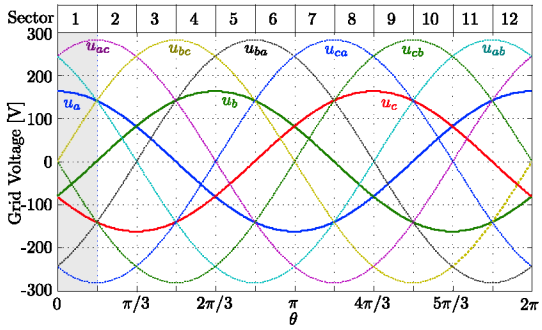

Figure 3: Sectors 1-12 of the mains phase voltage.

applied on the primary of the transformer in each switching cycle. There are five operation states: three active states (marked as time interval t_1, t_2 and t_3) and two freewheeling states (each with time interval of $t_4/2$). States 1, 3 and 5 are active states where each phase current is demanded proportionally to its corresponding phase voltage over one switching period, shown as $i_{rec,a}$, $i_{rec,b}$ and $i_{rec,c}$ in Fig. 4. Also the driven signals for the switches S_1, S_2, S_3, S_4 and the current injection switch S_{y2} are shown in Fig. 4. Driven signals for S_{y1} and S_{y3} are not shown in Fig. 4 because they are totally off in sector 1. Also, for explicit illustration, the current path for above mentioned five operation states is depicted in Fig. 5 a)-e) respectively.

By the functionality of the three-phase diode bridge $D_{N+/-}$, point P always presents the most positive voltage among the three phases, and likewise the most negative voltage at point N. Specifically in the presumed sector 1, D_{a+} and D_{c-} are always forward biased, which means that u_a is applied at point P and u_c at point N. During time interval t_1, S_3 and current injection switch S_{y2} are on, thus the voltage $u_a - u_b$ is applied on the primary of the transformer. $i_{rec,a}$ shows a discrete positive current with dc level of $I_{dc}\frac{N_2}{N_1}$ (I_{dc} is the output dc inductor current which is assumed constant in one switching period). Meanwhile the current circulates back through the injection path to phase B as $i_{rec,b}$. Next for the freewheeling time $t_4/2$, current injection switch S_{y2} is off and S_1 is on, resulting to a zero voltage on the primary of the transformer. Thus no currents are demanded from the mains and meanwhile output inductor current is freewheeling through the diode bridge on the secondary. In time interval t_2, S_4 is on after S_3 is turned off, thus a negative voltage is applied on the primary of the transformer with the value of $-(u_a - u_c)$. Consequently, $i_{rec,a}$

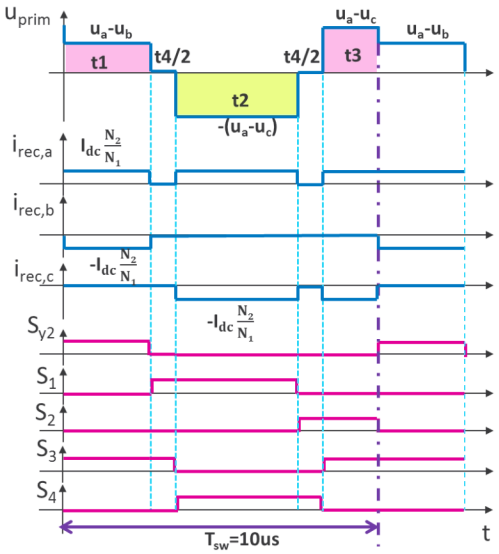

Figure 4: Operating principle of the proposed IS^{2}FBCIP Rectifier.

presents again a discrete positive current of $I_{dc}\frac{N_2}{N_1}$ while $i_{rec,c}$ shows a negative $-I_{dc}\frac{N_2}{N_1}$ correspondingly. At the following freewheeling time $t_4/2$, S_1 is turned off and then S_2 is turned on. Same like before, zero voltage applied on the primary of the transformer thus there is no direct power transfer between primary and secondary. Time interval t_3 is the last state in a switching period, where a reverse voltage of the one in t_2 is applied on the transformer, aiming at balancing the flux in the transformer over one switching period. Namely in the waveform of u_{prim}, the integral area over time intervals t_1 and t_3 has to be equal to the area of t_2. After time interval t_3, starts again the current injection state t_1 for the next period.

Since this topology is also a buck-type rectifier topology, the definition of modulation index M in [9] is still valid here. Thus, there is:

$$M = \frac{2}{3} \cdot \frac{N_1}{N_2} \cdot \frac{u_{out}}{\hat{U}_N} \tag{1}$$

where u_{out} represents the dc output voltage and $\hat{U}_N$ represents the amplitude of the input phase voltages.

B. Modulation Method

The modulation method is the essence of the performance for the proposed rectifier topology. Two principle laws have to be satisfied while designing the modulation method:

- Transformer volt-second balance,
- Ohmic behavior for each phase (under the condition of no reactive power handling).

To ensure the transformer volt-second balance, the magnetizing flux increment and decrement have to be equalized over one switching period. This implies that (e.g. in sector 1),

$$(u_a - u_b) \cdot t_1 + (u_a - u_c) \cdot t_3 = (u_a - u_c) \cdot t_2 \tag{2}$$

which derives

$$t_2 - t_3 = \frac{u_a - u_b}{u_a - u_c} \cdot t_1. \tag{3}$$

Besides, for the most negative phase C in this sector 1, according to the desired phase ohmic behavior, there is:

$$t_2 + t_3 = \frac{M}{\hat{U}_N} \cdot |u_c| \cdot T_{sw}. \tag{4}$$

Meanwhile to maintain ohmic behavior for the intermediate phase by current injection (i.e. phase B in sector 1),

$$t_1 = \frac{M}{\hat{U}_N} \cdot |u_b| \cdot T_{sw} \tag{5}$$

can be obtained. Combining (3) and (4), there is:

$$t_2 = \frac{1}{2}\left(\frac{M}{\hat{U}_N} \cdot |u_c| + \frac{u_a - u_b}{u_a - u_c} \cdot \frac{M}{\hat{U}_N} \cdot |u_b|\right) \cdot T_{sw} \tag{6}$$

and

$$t_3 = \frac{1}{2}\left(\frac{M}{\hat{U}_N} \cdot |u_c| - \frac{u_a - u_b}{u_a - u_c} \cdot \frac{M}{\hat{U}_N} \cdot |u_b|\right) \cdot T_{sw}. \tag{7}$$

In the end, the total freewheeling time can be calculated as

$$t_4 = T_{sw} - t_1 - t_2 - t_3 \tag{8}$$

and each $t_4/2$ will be placed between two active states.

Thus, according to Fig. 4, duty cycle for all the switches in sector 1 can be obtained:

$$d_{S_{y2}} = t_1/T_{sw} \tag{9}$$

$$d_{S_1} = (t_2 + \frac{1}{2}t_4)/T_{sw} \tag{10}$$

$$d_{S_2} = (t_3 + \frac{1}{2}t_4)/T_{sw} \tag{11}$$

$$d_{S_3} = (t_1 + t_3 + \frac{1}{2}t_4)/T_{sw} \tag{12}$$

$$d_{S_4} = (t_2 + \frac{1}{2}t_4)/T_{sw} \tag{13}$$

C. Zero Voltage Switching

By the merit of the full-bridge architecture, the presence of leakage inductance in the transformer enables soft-switching for each switching transition, this almost eliminates all switching losses above certain load level [8]. In [8], ZVS is only realized in the DC/DC full-bridge stage, but not in the injection circuit. However in this proposed topology, the functionality of current injection is integrated into the full-bridge operation inside every switching period, thus all the bidirectional switching pairs (S_{y1}, S_{y2} and S_{y3}) on current injection path can also realize ZVS.

As discussed in [10], for leading leg switches S_1 S_2 and S_y, at the moment before its turn-on, it is always in an active state where the energy used to charge or discharge its output capacitance is the energy stored in the L_{lk} plus the energy stored in the output filter inductor L_o. Since the energy in L_o is quite large compared to the energy needed to charge the

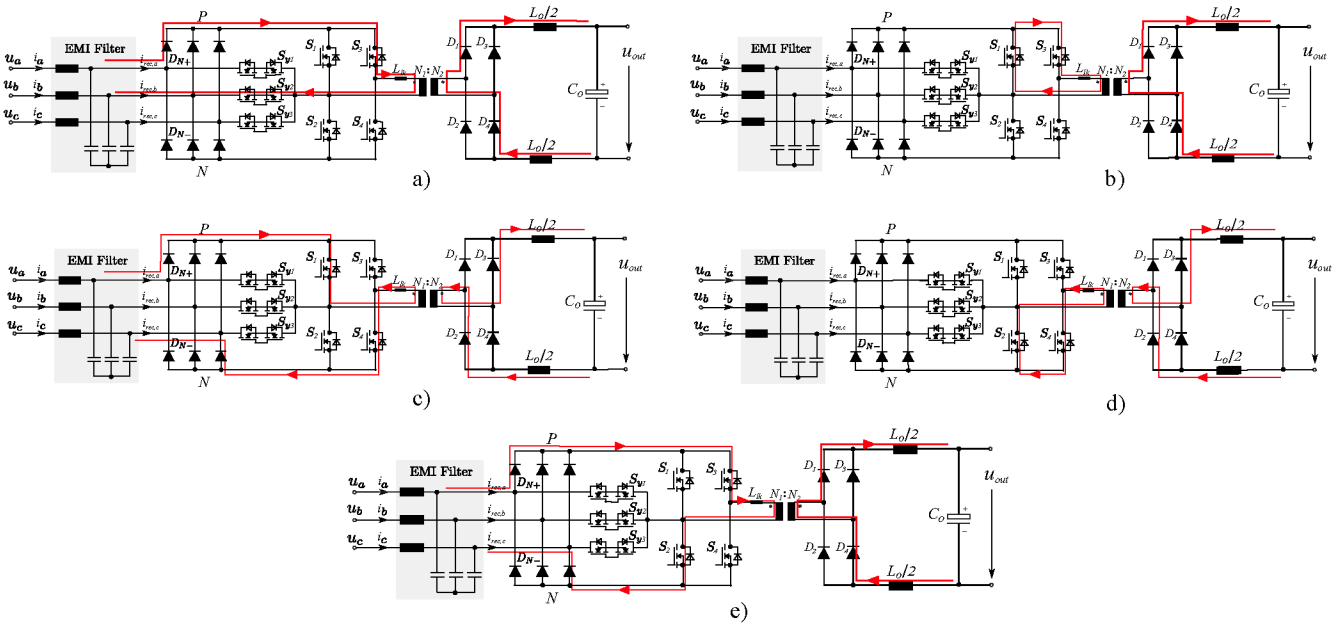

Figure 5: Current path at five different operation states inside one switching cycle in sector 1.

output capacitance, it can be considered to charge as a constant current on MOSFET C_{oss}. And the charging current $I_{p,max}$ corresponds to the peak value of output inductor current ripple reflected to the primary, i.e:

$$I_{p,max} = I_{L,max} \cdot \frac{N_2}{N_1} \tag{14}$$

and the most strict moment to achieve ZVS regarding u_{DS} is the moment when the maximum line-to-line voltage reaches its peak:

$$U_{DS,max} = \sqrt{3}\hat{U}_N. \tag{15}$$

For a more precise analysis, the non-linear behavior of MOSFET C_{oss} should be considered. Thus the minimum deadtime applied on leading leg switches (δ_1) can be obtained by

$$2\int_0^{U_{DS,max}} C_{oss}(u_{DS}) \cdot d(u_{DS}) = I_{p,max} \cdot \delta_1. \tag{16}$$

The left part can be easily achieved by integrating the area below the provided C_{oss}-u_{DS} curve in MOSFET device datasheet.

on the other hand, the turn-on of the lagging leg switches S_3 S_4 happens after a freewheeling state, which means that only the energy stored in the L_{lk} is available for charging or discharging its C_{oss}. Then the energy stored in L_{lk} has to comply

$$E = \frac{1}{2}L_{lk}I_{p2}^2 = \int_0^{U_{DS,max}} C_{oss}(u_{DS}) \cdot d(u_{DS}^2) \tag{17}$$

where I_{p2} is the primary current at turn-on moment of the lagging leg switch which has

$$I_{p2} = (I_{L,max} - \frac{u_{out}}{L_o}\frac{t_4}{2}) \cdot \frac{N_2}{N_1}. \tag{18}$$

Thus, the resonance between L_{lk} and C_{oss} provides a sinusoidal voltage rise across the switch to be turned on. Thus the deadtime for the lagging leg switches (δ_2) should be at one fourth of the resonant period

$$\delta_2 = \frac{T_{res}}{4} = \frac{\pi}{2}\sqrt{L_{lk}C_{oss}}. \tag{19}$$

The simulation result showing the ZVS behavior of one switching period in sector 1 is depicted in Fig. 6. Proper deadtime has been applied to the driven signals of S_1, S_2, S_3, S_4, S_{y2+} (the left one of bidirectional switches pair S_{y2}) and S_{y2-} (the right one of S_{y2}). The shaded area implies all the five switching transitions, one can see that each switch starts to conduct current through the channel while its drain-source voltage reaches zero. A detailed zoom-in shows the MOSFET non-linear C_{oss} charging/discharging characteristic.

III. Converter Design

The application of the proposed rectifier topology is rooted in avionic utilities, thus in order to build a demonstrator prototype, the design specification and requirements are shown in Table I.

A. Stresses on the Switches

The transistors in this topology can be classified into two groups: those switching at high frequency (i.e. switching frequency), and those switching at an equivalently intermediate frequency between mains frequency and switching frequency. The full-bridge switches (S_1, S_2, S_3, S_4) are always switching at switching frequency, and the bidirectional switching pairs on current injection path (S_{y1}, S_{y2} and S_{y3}) are only switching during the sectors where its corresponding phase voltage has the minimum absolute value. The voltage stress on the full-bridge switches has an envelope of maximal line to line voltage, which gives peak voltage stress:

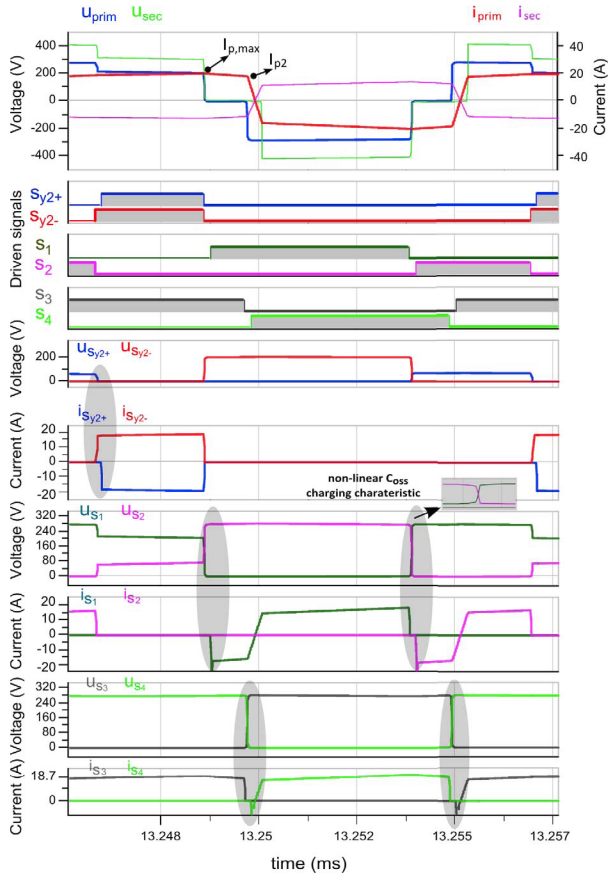

Figure 6: ZVS realization of one switching period in sector 1.

Table I: Design specifications and requirements of the proposed isolated single-stage three-phase PFC Rectifier with current injection path

Parameter	Value
Galvanic Isolation	Yes
Input three-phase voltage	115V$_{rms,l-n}$
Mains frequency	400Hz
Power Factor	$\geq 95\%$
THD	$\leq 5\%$
Switching frequency	100kHz
Output voltage	270V
Output power rated	3.3kW
Semiconductor voltage derating	75%
Electrolytic capacitors	Not allowed
Temperature derating	70%

$$\hat{u}_{S1,2,3,4} = \sqrt{3} \cdot \hat{U}_N. \tag{20}$$

The highest voltage stress on the switches in current injection path occurs at the moment when one phase voltage reaches its maximum amplitude and the other two are equal to half of the maximum amplitude, resulting in:

$$\hat{u}_{Sy1,2,3} = \frac{3}{2} \cdot \hat{U}_N. \tag{21}$$

Regarding the current stress, the behavior of the two legs (leg S_1 and S_2, leg S_3 and S_4) are not the same because: S_3 and S_4 are always conducting current alternatively inside each switching cycle; while S_1 and S_2 are not, since S_1, S_2 together with current injection path S_y are conducting current alternatively inside every switching cycle.

The average and RMS currents through the switches on current injection path over one mains period are derived respectively:

$$I_{Sy1,2,3,RMS} = \sqrt{\frac{(2-\sqrt{3})M}{2\pi}} \cdot \frac{N_2}{N_1} I_{dc}. \tag{22}$$

Thus, average and RMS currents through the switches S_1 and S_2 are derived:

$$I_{S_{1,2},RMS} = \sqrt{\frac{3}{\pi}(0.5236 - 0.134M)} \cdot \frac{N_2}{N_1} I_{dc}. \tag{23}$$

Since S_3 and S_4 are alternatively sharing the current $\frac{N_2}{N_1} I_{dc}$ inside every switching cycle, also its on-time is symmetrical during every 30°-sector, which yields to the RMS currents of S_3 and S_4:

$$I_{S_{3,4},RMS} = \frac{\sqrt{2}}{2} \cdot \frac{N_2}{N_1} I_{dc}. \tag{24}$$

B. Input and Output Diode Rectifier

The three-phase diode bridge D_{N+} and D_{N-} are low frequency devices which switch at mains frequency. The voltage stress on the three-phase diode rectifier is equal to the maximal line-to-line input voltage, giving the highest voltage stress:

$$\hat{u}_{D_{N\pm}} = \sqrt{3} \cdot \hat{U}_N. \tag{25}$$

Thus, Si-diodes with a low forward voltage drop and a blocking voltage of at least 400 V should be selected.

The output diode rectifier is working at switching frequency, and its voltage stress corresponds to the voltage stress in the low frequency input diodes multiplied by the turns-ratio of the transformer, which is,

$$\hat{u}_{D1,2,3,4} = \frac{N_2}{N_1} \cdot \sqrt{3} \cdot \hat{U}_N. \tag{26}$$

Regarding the current stress, the average and RMS currents through the three-phase diode bridge are respectively given by:

$$I_{D_{N\pm},avg} = \frac{\sqrt{3}M}{2\pi} \cdot \frac{N_2}{N_1} I_{dc} \tag{27}$$

$$I_{D_{N\pm},RMS} = \sqrt{\frac{\sqrt{3}M}{2\pi}} \cdot \frac{N_2}{N_1} I_{dc}. \tag{28}$$

The current through the output diode rectifier is related with the current through full-bridge switches S_3 and S_4, thus its average and RMS currents are respectively given by:

$$I_{D_{1,2,3,4},avg} = \frac{1}{2} \cdot I_{dc} \tag{29}$$

$$I_{D_{1,2,3,4},RMS} = \frac{\sqrt{2}}{2} \cdot I_{dc}. \tag{30}$$

C. Transformer

The transformer is one of the most important components in the proposed topology, since the modulation of the rectifier is tightly connected to the presence of the transformer. This is different from the proposed I^{2}AFM PFC Rectifier in [8], where the functionality of the full-bridge stage is decoupled from the rectifier stage with a capacitor in between. Besides, based on the desired ZVS feature, the leakage inductance L_{lk} of the transformer has to be decided in order to achieve a certain ZVS range.

The shape of the transformer primary voltage inside one switching cycle of sector 1 is illustrated as u_{prim} in Fig. 4. Even though in state 1 voltage stress on transformer is smaller compared to states 3 and 5, the maxim flux density $\hat{B}$ is defined when the primary voltage reaches peak value of the maximum line-to-line voltage, i.e. $\theta = \frac{n\pi}{6}$(n=1, 3, 5...). Also at these moments, time interval for state 1 (t_1 in Fig. 4) equals to zero since the average current demanded by the phase with minimum absolute value will be 0. Therefore, time interval for state 3 (t_2 in Fig. 4) and state 5 (t_3 in Fig. 4) will be equal. Thus the rectifier will work like a classical phase-shifted full-bridge [10] which gives the maximum flux density:

$$\hat{B} = \frac{\sqrt{3}\hat{U}_N \cdot T_{sw}/2}{N_1 \cdot A_{core}} \tag{31}$$

where A_{core} represents the cross section area of the chosen core.

Also based on (1), the turns ratio of the transformer can be represented:

$$N_1/N_2 = \frac{3}{2} \cdot M_{max} \cdot \frac{\hat{U}_N}{u_{out}}. \tag{32}$$

Usually maximum modulation index M_{max} for nominal output power is set around 0.9 to leave enough margin for the control [11] and also take into consideration of the duty cycle loss from applied duty cycle on the primary to the effective duty cycle on the secondary for full-bridge topology [10].

To achieve ZVS, Sufficient leakage inductance L_{lk} as discussed in Section II-C can be achieved by adding insulator between primary winding and secondary winding. Finally the transformer winding construction is described in Table II, which after measurement shows magnetizing inductance L_{mag}=1.2 mH and leakage inductance L_{lk}=2.8 uH on primary side.

D. Input and Output Filter

The input filer has to be designed in a way that the EMC measurement complies with the military standard MIL-STD-461E [12], this imposes more difficulty in input filter design compared to CISPR standard [13] in industrial application. In CISPR standard, the EMI spectrum has limit in the range of 150 kHz-30 MHz, thus the switching frequency can be chosen below 150 kHz with the grid frequency being 50/60 Hz so that the current spectral component at switching frequency (or even the first several harmonics of switching frequency) doesn't have to be considered for the input filter design [11]. However, in MIL-STD-461E, the limit starts from 10 kHz (see Fig. 8) which is much smaller compared to the starting frequency of

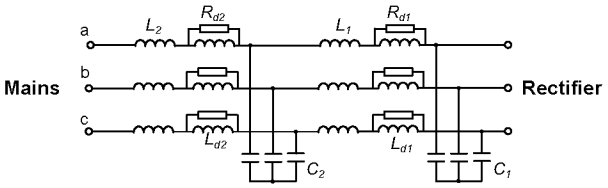

Figure 7: Circuit diagram of the two-stage input EMI filter.

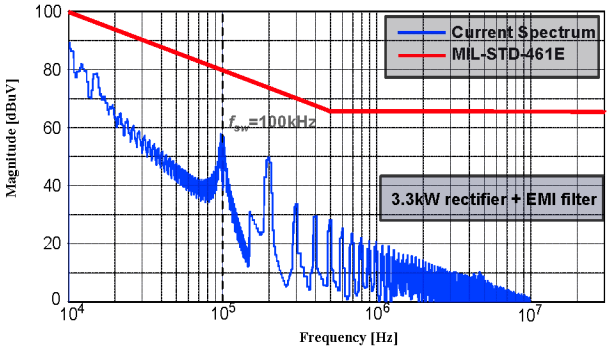

Figure 8: Input Current Spectrum of the 3.3kW IS^{2}FBCIP PFC Rectifier (complying with the MIL-STD-461E standard).

CISPR, meanwhile being closer to the mains frequency (400 Hz). Therefore, the switching frequency has to be placed inside the MIL-STD-461E frequency range and moreover, the EMI filter has to be designed to attenuate the first harmonic of switching frequency.

Furthermore, buck-type rectifiers feature pulsating input currents, thus compared to boost-type rectifiers, more EMI filter effort is needed. Shown in Fig. 7, a two-stage filter with $R - L_d$ series damping [14] is employed, noting that the first stage filter capacitors C_1 have to placed closely to the rectifier input stage in order to maintain a low commutation inductance [11].

Output filter $L_o - C_o$ can be designed based on dc inductor current ripple and output voltage ripple values. Assuming that the output voltage (u_{out}) ripple is negligible accross C_o, the maximum inductor current ripple happens at moments $\theta = \frac{n\pi}{6}$(n=1, 3, 5...) where the phase with intermediate voltage value is crossing zero thus no current demanded from current injection path, which gives the maximum inductor current ripple value:

$$\Delta i_{L,pp,max} = \frac{u_{out} \cdot (1 - \frac{\sqrt{3}}{2}M)}{2 \cdot f_{sw} \cdot L_o} = \frac{3M\hat{U}_N}{4L_o f_{sw}} \frac{N_2}{N_1}(1 - \frac{\sqrt{3}}{2}M). \tag{33}$$

E. Simulation Results

Since the proposed rectifier is a PWM buck-type rectifier, it demands a pulsating input current from the mains [5]. Consequently an EMI input filter is is deisgned to make the demanded current comply with military standard MIL-STD-461E [12]. Performed in simulator GeckoCIRCUITS [15], LISN (Line Impedance Stabilization Network) measurement of the input current spectrum in comparison with MIL-STD-461E is shown in Fig. 8. It can be seen that the designed EMI filter for this 3.3kW rectifier can comply with MIL-STD-461E.

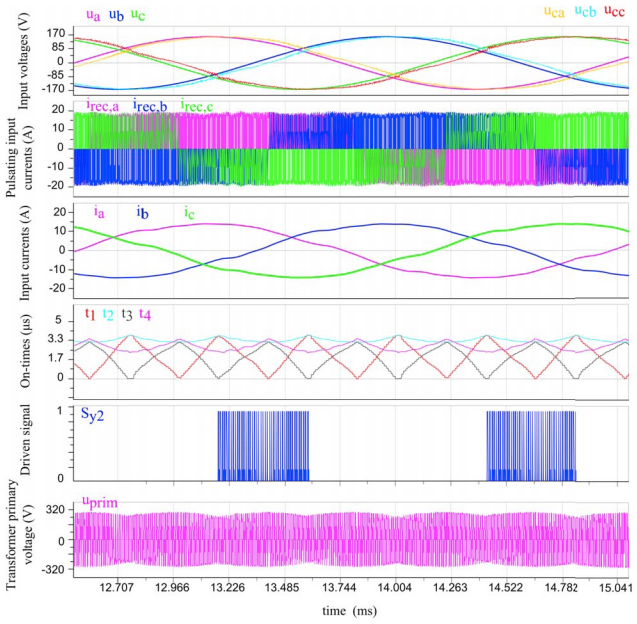

Figure 9: Simulated waveforms of the proposed IS^{2}FBCIP PFC Rectifier.

A simulation result of the overall performance of the rectifier with its EMI filter is shown in Fig. 9, working at $P_{o,nom}$=3.3 kW, N_1/N_2=1/1.5, M=0.8 together with input and output filter value listed in Table II. One can see that, according to three-phase voltages at the input capacitors of the rectifier (u_{ca}, u_{cb} and u_{cc}), a three-phase pulsating current ($i_{rec,a}$, $i_{rec,b}$ and $i_{rec,c}$) are demanded by the modulation scheme of the rectifier, which is in phase with capacitor voltages. Input currents from the mains are filtered by the EMI filter placed before the rectifier, thus three-phase currents (i_a, i_b and i_c) show good THD and PF with respect to u_{ca}, u_{cb} and u_{cc}. Times intervals t_1, t_2, t_3 and t_4 are discussed in II-B, it is obvious that t_1 shows a third-harmonic behavior which indicates the on-time of the third-harmonic injection switching pairs. Driven signal S_{y2} on third-harmonic injection path is active only when phase B carries the minimum absolute voltage. Voltage across the transformer primary side (u_{prim}) shows switching characteristic and also with an enveloped of maximum line-to-line voltage defined by the three-phase diode bridge.

IV. Prototype Design

In order to validate the design of the rectifier system, a 3.3kW rectifier including EMI filter has been designed. Key components like semiconductors have been chosen, also the transformer and inductors have been designed, wound and measured. Design of the mechanical layout is in the process. The control stage is implemented by a TMS320F28377D dual-core microcontroller. A list of the main components is provided in Table. II, with the corresponding losses estimation listed in Fig. 10. It shows an overall efficiency of 95.1%, which is moderate compared to the state-of-the-art rectifier topologies with isolation [5], [8], [11]. This is due to the stricter military EMI standard and also the semiconductor voltage and temperature derating applied according to Table I.

Table II: List of component employed in the prototype of the proposed isolated single-stage three-phase PFC Rectifier with current injection path

Component	Description
L_1=L_2=200 μH	3 stacked toroid powder cores 58547, N=22, solid wire of 1 mm diameter 4 in parallel
C_1=C_2=3 μF	2X1.5 μF B32923 (305V ac) film capacitor
L_{d1}=L_{d2}=100 μH	1 toroid powder core 58548, N=29, solid wire of 0.9 mm diameter 4 in parallel
R_{d1}=R_{d2}=25 Ω	CRCW251224R9 (1W) thick film SMD resistor
Input diodes D_{N+} D_{N-}	400 V/30 A STTH30R04 ultra fast recovery diode
Current injection path S_{y1-3}	650 V CoolMOS C6 series (IPW65R037C6)
Full-bridge S_{1-4}	650 V CoolMOS C7 series (IPW65R045C7)
Output diodes D_{1-4}	1200 V/43 A C4D30120D SiC Schottky diode
Transformer	Ferrite core PM87 material N27, N_1/N_2=10/15, primary Litz wire 200X0.07 mm 10 in parallel, insulator material Kapton of horizontal width 6.5 mm, secondary Litz wire 200X0.07 mm 4 in parallel
Output inductor L_o=2X100 μH	Ferrite core ETD59 material N87, airgap 1.2 mm, 15 turns, solid wire of 1.2 mm diameter 8 in parallel
Output capacitor C_o=200 μF	5X40 μF B32776 (450V dc) film capacitor

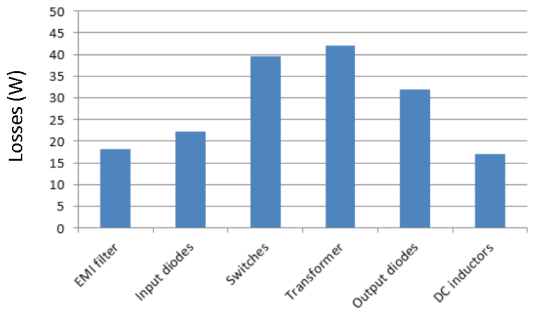

Figure 10: Distribution of losses estimation for the prototype design at $P_{o,nom}$=3.3 kW

V. Conclusion

This paper presented a new isolated single-stage three-phase full-bridge with current injection path PFC rectifier (denominated as IS^{2}FBCIP PFC Rectifier). Its operating principle, modulation method and ZVS feature have been discussed and the difference regarding I^{2}AFM PFC rectifier has been addressed. Also a design guideline and simulation results are provided to validate the functionality of the proposed topology. Main components in the experimental prototype is decided. This IS^{2}FBCIP PFC Rectifier features an indirect matrix type converter, which is an integration of three-phase diode bridge with current injection path and a full-bridge stage without intermediate energy storage capacitor. The major advantages of the IS^{2}FBCIP PFC Rectifier are

the relatively low number of switching components, low implementation effort and its ZVS feature which leads to a high overall efficiency.